

HRLO110N03K

30V N-Channel Trench MOSFET

Features

- Low Dense Cell Design, Logic Level
- Reliable and Rugged
- Advanced Trench Process Technology
- 100% UIS Tested, 100% Rg Tested
- Lead free, Halogen Free

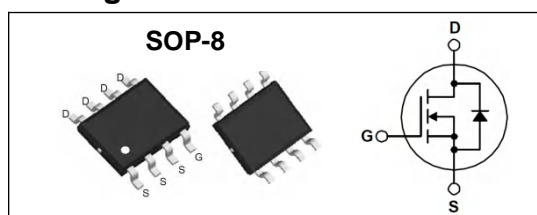
Application

- Power Management in Inverter System
- Synchronous Rectification

Key Parameters

Parameter	Value	Unit
BV_{DSS}	30	V
I_D	13.8	A
$R_{DS(on)}$, typ @10V	9.0	m Ω
$R_{DS(on)}$, typ @4.5V	13.0	m Ω

Package & Internal Circuit



Absolute Maximum Ratings $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units	
V_{DSS}	Drain-Source Voltage	30	V	
V_{GS}	Gate-Source Voltage	± 20	V	
I_D	Drain Current	$T_A = 25^\circ\text{C}$	13.8	A
		$T_A = 100^\circ\text{C}$	8.7	A
I_{DM}	Pulsed Drain Current	55	A	
E_{AS}	Single Pulsed Avalanche Energy	L=1mH	210	mJ
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	3.1	W
		$T_A = 70^\circ\text{C}$	2.0	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$	

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Lead	--	24	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient ($t \leq 10\text{s}$)	--	40	$^\circ\text{C}/\text{W}$
	Junction-to-Ambient (steady state)	--	75	$^\circ\text{C}/\text{W}$

Electrical Characteristics $T_J=25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

On Characteristics

V_{GS}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	--	3.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 13\text{ A}$	--	9.0	11.0	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	--	13.0	15.6	m Ω

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 24\text{ V}, T_J = 125\text{ }^\circ\text{C}$	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	± 100	nA

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	--	1170	--	pF
C_{oss}	Output Capacitance		--	165	--	pF
C_{rss}	Reverse Transfer Capacitance		--	105	--	pF
R_g	Gate Resistance	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ V}, f = 1\text{ MHz}$	--	1	--	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Time	$V_{DS} = 15\text{ V}, I_D = 13\text{ A}, R_G = 6\text{ }\Omega$	--	12	--	ns
t_r	Turn-On Rise Time		--	10	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	55	--	ns
t_f	Turn-Off Fall Time		--	15	--	ns
$Q_{g(10V)}$	Total Gate Charge	$V_{DS} = 24\text{ V}, I_D = 13\text{ A}, V_{GS} = 10\text{ V}$	--	21	--	nC
$Q_{g(4.5V)}$	Total Gate Charge		--	10	--	nC
Q_{gs}	Gate-Source Charge		--	5.4	--	nC
Q_{gd}	Gate-Drain Charge		--	2.8	--	nC

Source-Drain Diode Characteristics

V_{SD}	Source-Drain Diode Forward Voltage	$I_S = 13\text{ A}, V_{GS} = 0\text{ V}$	--	--	1.3	V
t_{rr}	Reverse Recovery Time	$I_S = 20\text{ A}, V_{GS} = 0\text{ V}, di_F/dt = 100\text{ A}/\mu\text{s}$	--	23	--	ns
Q_{rr}	Reverse Recovery Charge		--	15	--	nC

Typical Characteristics

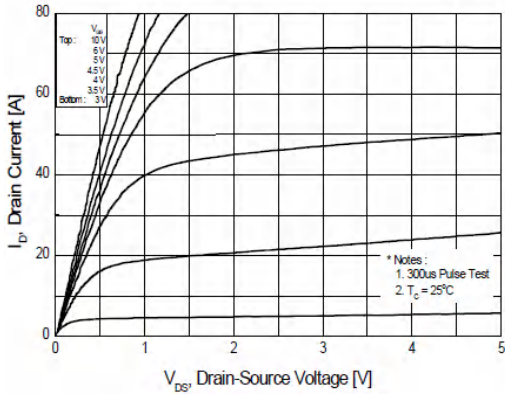


Figure 1. On Region Characteristics

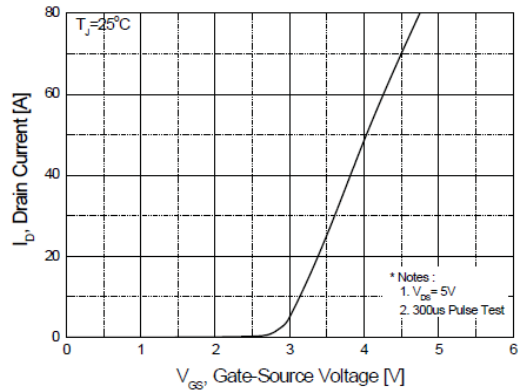


Figure 2. Transfer Characteristics

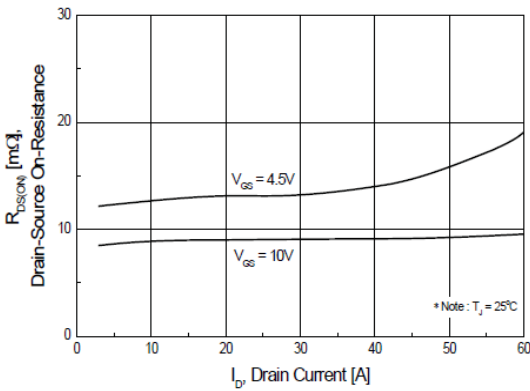


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

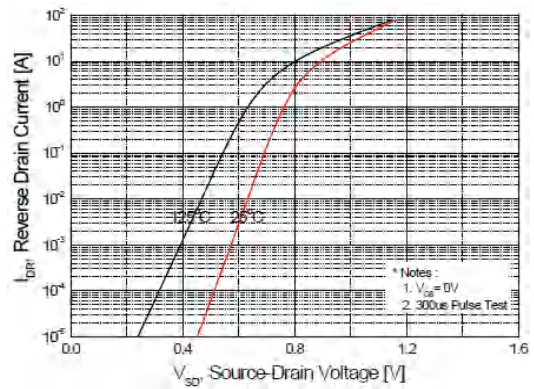


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

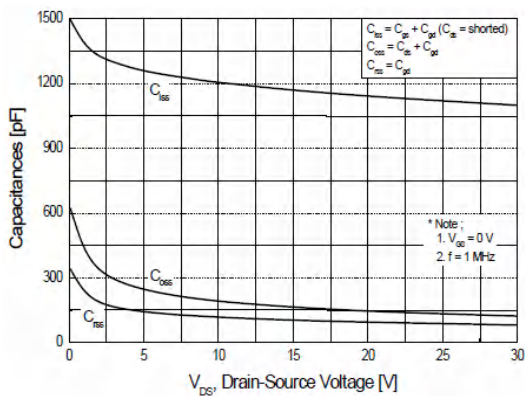


Figure 5. Capacitance Characteristics

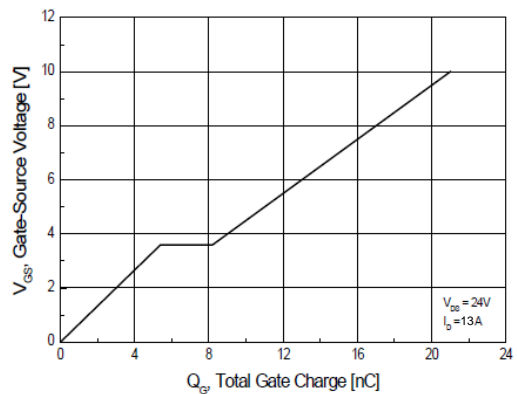


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

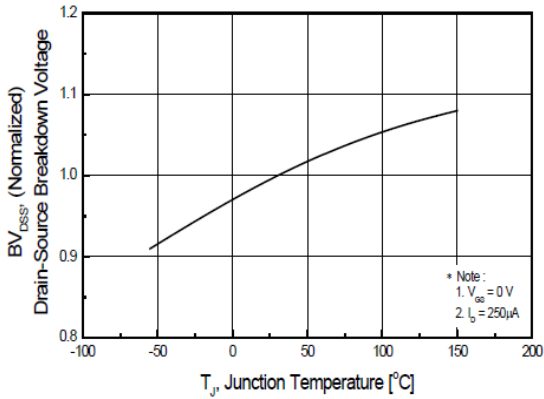


Figure 7. On-Resistance Variation vs Gate-Source Voltage

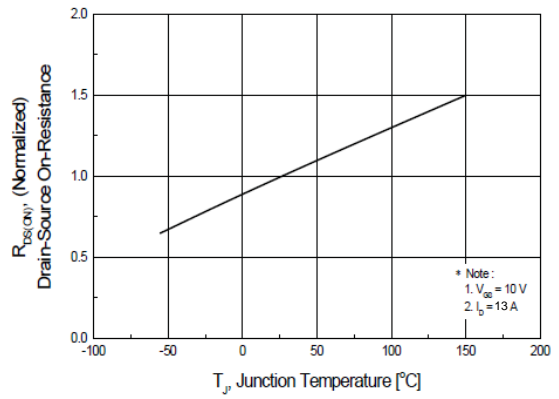


Figure 8. On-Resistance Variation vs Temperature

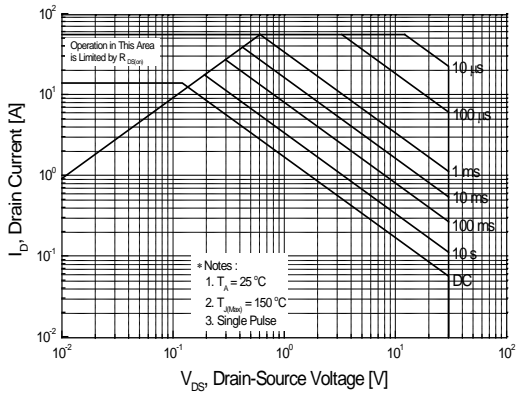


Figure 9. Maximum Safe Operating Area

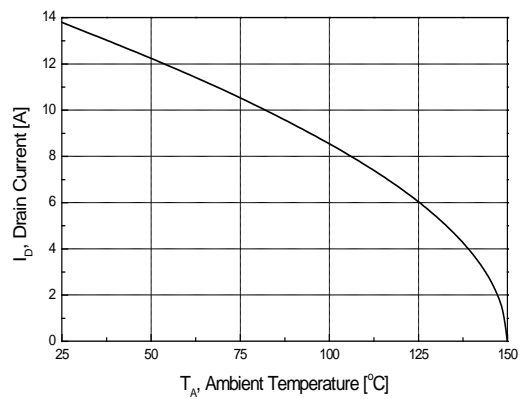


Figure 10. Maximum Drain Current vs Case Temperature

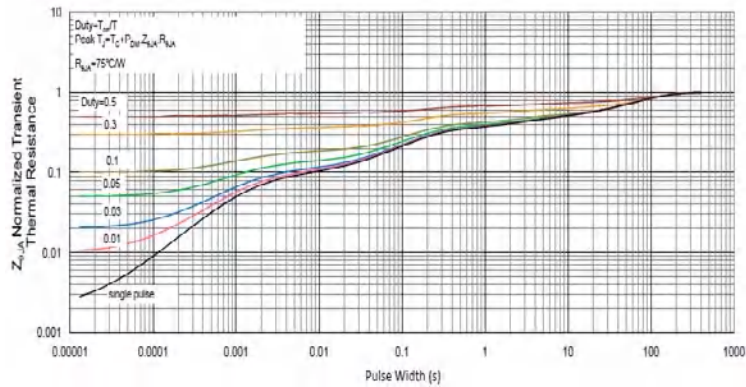


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform



Fig 13. Resistive Switching Test Circuit & Waveforms

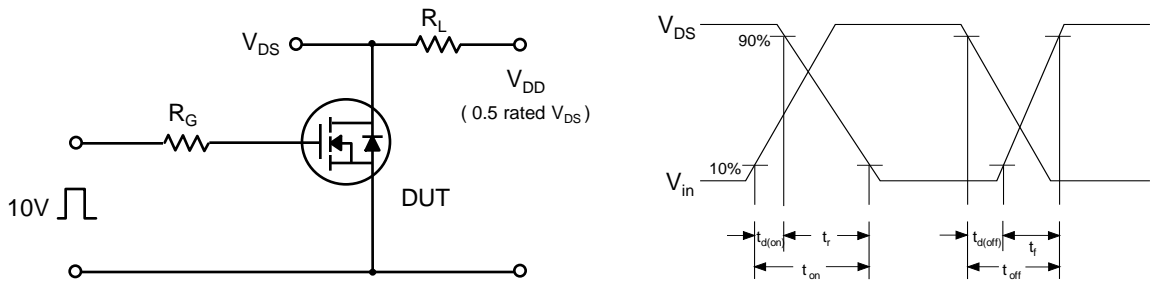


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

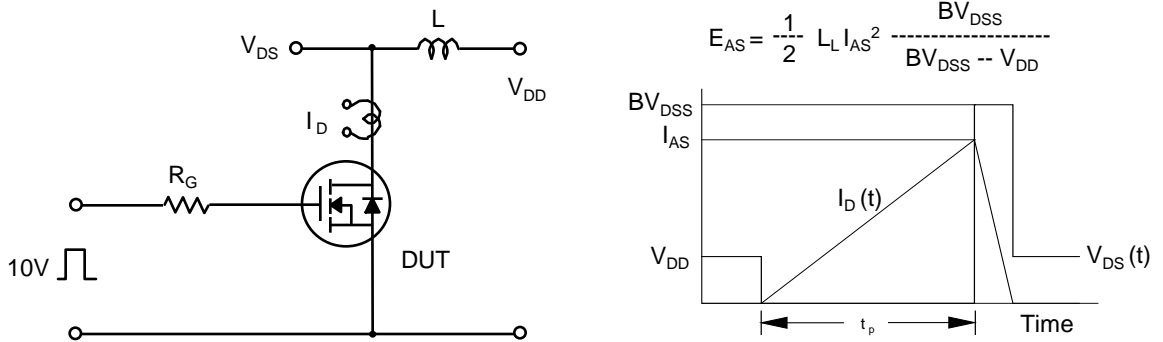
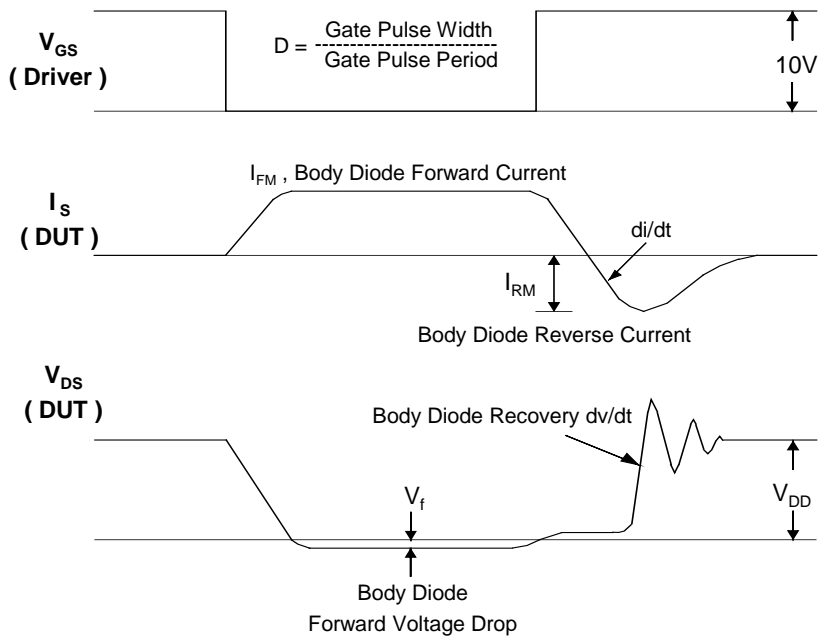
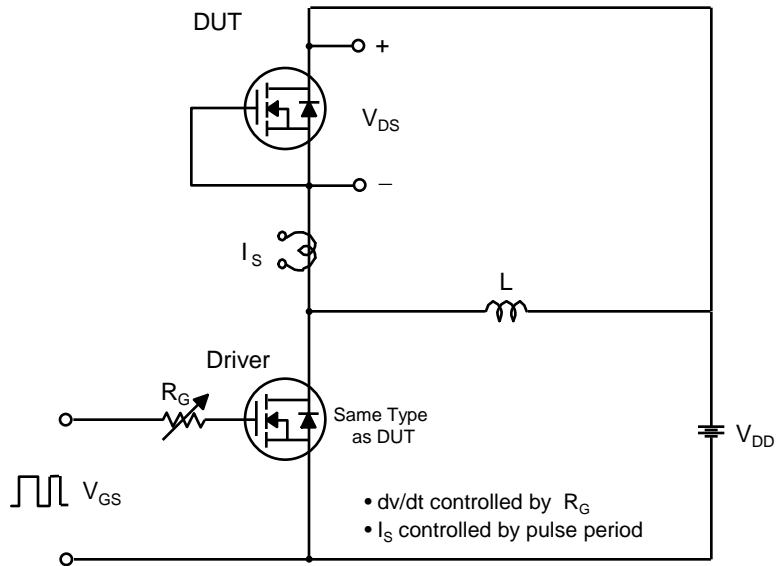


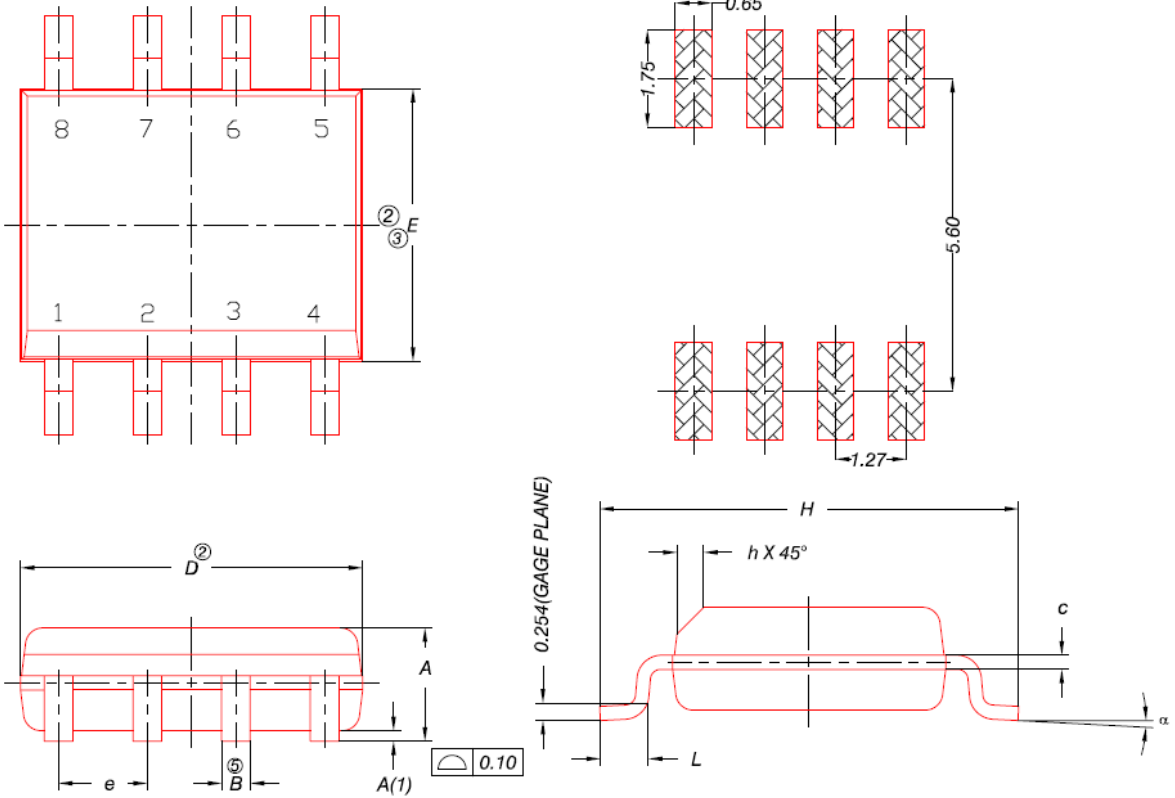
Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

SOP-8

Land Pattern
(Only for Reference)



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.35	1.55	1.75
A(1)	0.10	0.18	0.25
B	0.38	0.45	0.51
C	0.19	0.22	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
e	1.27 BSC		
H	5.80	6.00	6.20
L	0.50	0.72	0.93
α	0°	4°	8°
h	0.25	0.38	0.50