

HRD85N08K

80V N-Channel Trench MOSFET

Features

- Low Dense Cell Design
- Reliable and Rugged
- Advanced Trench Process Technology
- 100% UIS Tested, 100% Rg Tested

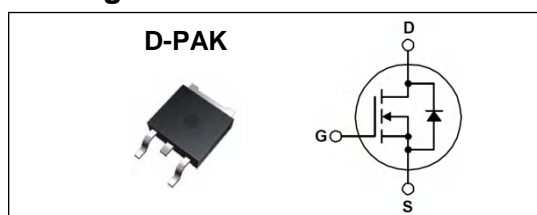
Application

- Power Management in Inverter System
- Synchronous Rectification

Key Parameters

Parameter	Value	Unit
BV_{DSS}	80	V
I_D (Silicon Limited)	110	A
$R_{DS(on), typ}$	7	m Ω

Package & Internal Circuit



Absolute Maximum Ratings $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units	
V_{DSS}	Drain-Source Voltage	80	V	
V_{GS}	Gate-Source Voltage	± 25	V	
I_D	Drain Current (Silicon Limited)	$T_C = 25^\circ\text{C}$	110	A
		$T_C = 100^\circ\text{C}$	77	A
	Drain Current (Package Limited)	$T_C = 25^\circ\text{C}$	70	A
I_{DM}	Pulsed Drain Current	385	A	
E_{AS}	Single Pulsed Avalanche Energy	$L=1\text{mH}$	290	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	200	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$	

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	0.75	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient (minimum pad of 2 oz copper)	--	110	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient (* 1 in ² pad of 2 oz copper)	--	50	$^\circ\text{C}/\text{W}$

Electrical Characteristics $T_J=25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
V_{GS}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.2	--	3.8	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\ \text{V}, I_D = 30\ \text{A}$	--	7.0	8.5	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 5\ \text{V}, I_D = 30\ \text{A}$	--	42	--	S
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\ \text{V}, I_D = 250\ \mu\text{A}$	80	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64\ \text{V}, V_{GS} = 0\ \text{V}$	--	--	1	μA
		$V_{DS} = 64\ \text{V}, T_J = 125\text{ }^\circ\text{C}$	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 25\ \text{V}, V_{DS} = 0\ \text{V}$	--	--	± 100	nA
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1.0\ \text{MHz}$	--	3200	--	pF
C_{oss}	Output Capacitance		--	440	--	pF
C_{rss}	Reverse Transfer Capacitance		--	270	--	pF
R_g	Gate Resistance	$V_{GS} = 0\ \text{V}, V_{DS} = 0\ \text{V}, f = 1\ \text{MHz}$	--	1.2	--	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	$V_{DS} = 40\ \text{V}, I_D = 30\ \text{A},$ $R_G = 6\ \Omega$	--	50	--	ns
t_r	Turn-On Rise Time		--	65	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	140	--	ns
t_f	Turn-Off Fall Time		--	50	--	ns
Q_g	Total Gate Charge	$V_{DS} = 64\ \text{V}, I_D = 30\ \text{A},$ $V_{GS} = 10\ \text{V}$	--	75	--	nC
Q_{gs}	Gate-Source Charge		--	20	--	nC
Q_{gd}	Gate-Drain Charge		--	25	--	nC
Source-Drain Diode Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage	$I_S = 30\ \text{A}, V_{GS} = 0\ \text{V}$	--	--	1.3	V
t_{rr}	Reverse Recovery Time	$I_S = 30\ \text{A}, V_{GS} = 0\ \text{V}$ $di_F/dt = 100\ \text{A}/\mu\text{s}$	--	45	--	ns
Q_{rr}	Reverse Recovery Charge		--	65	--	nC

Typical Characteristics

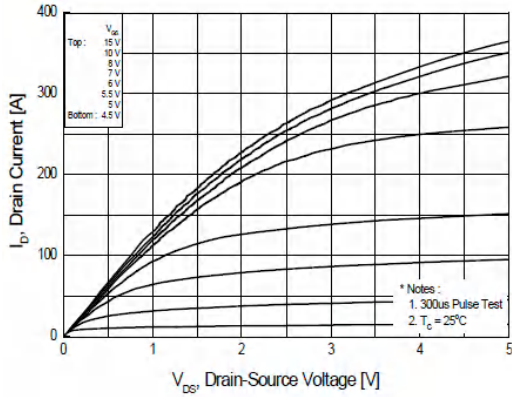


Figure 1. On Region Characteristics

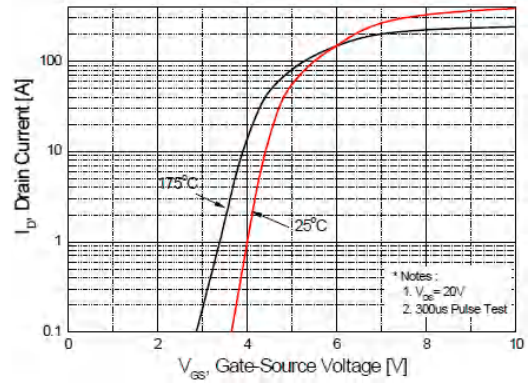


Figure 2. Transfer Characteristics

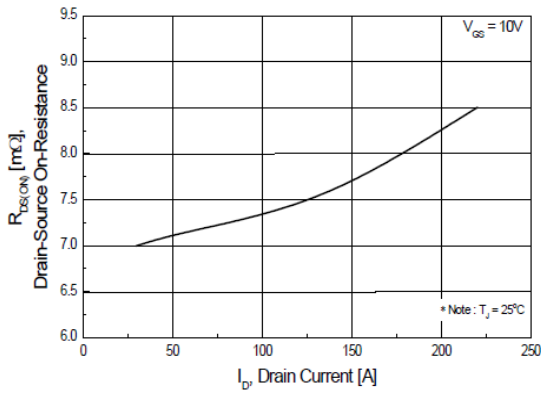


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

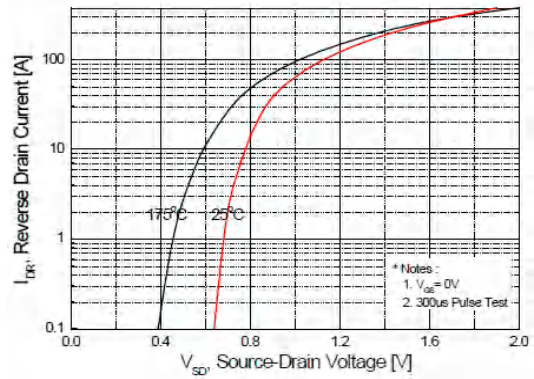


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

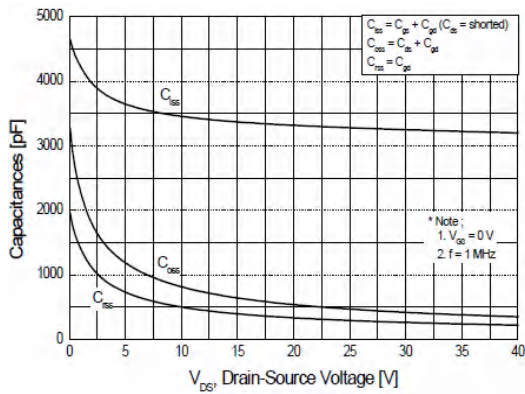


Figure 5. Capacitance Characteristics

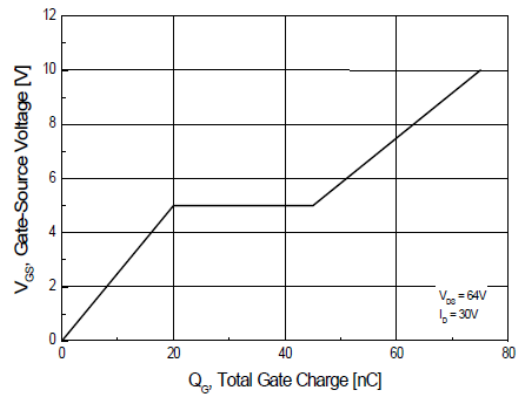


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

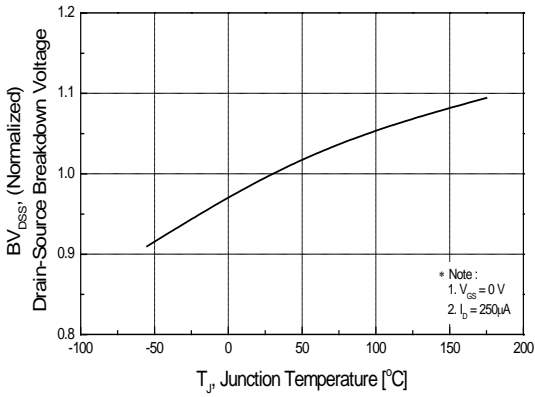


Figure 7. On-Resistance Variation vs Gate-Source Voltage

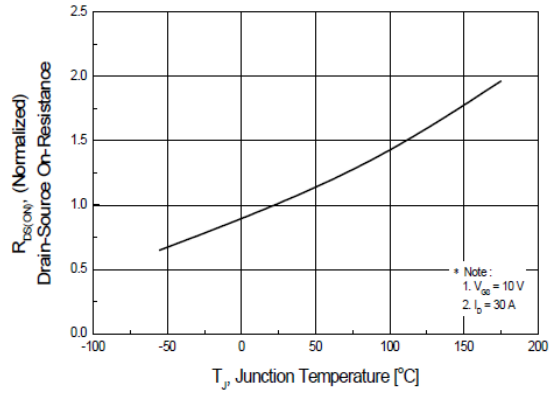


Figure 8. On-Resistance Variation vs Temperature

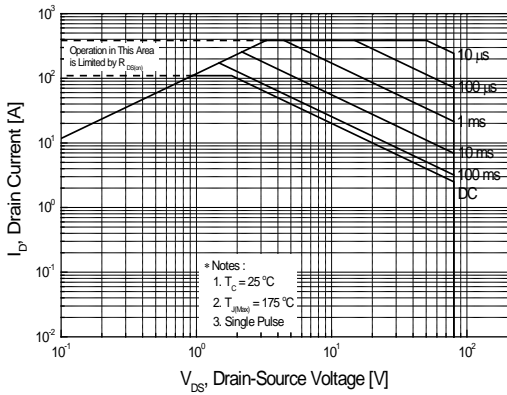


Figure 9. Maximum Safe Operating Area

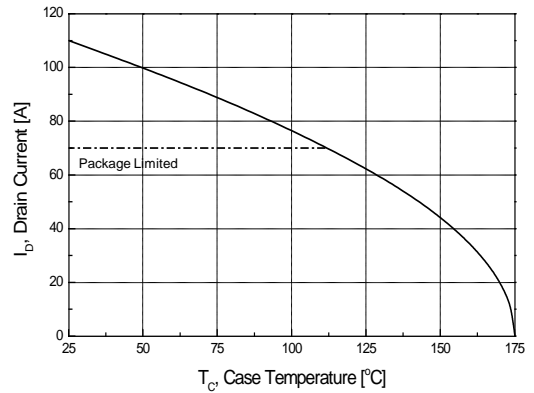


Figure 10. Maximum Drain Current vs Case Temperature

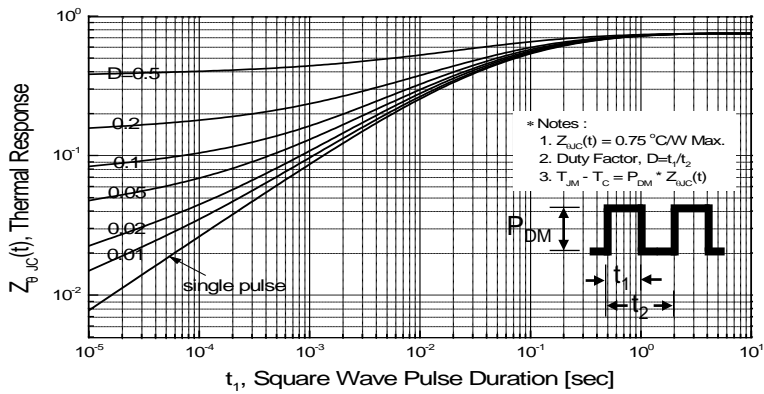


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform

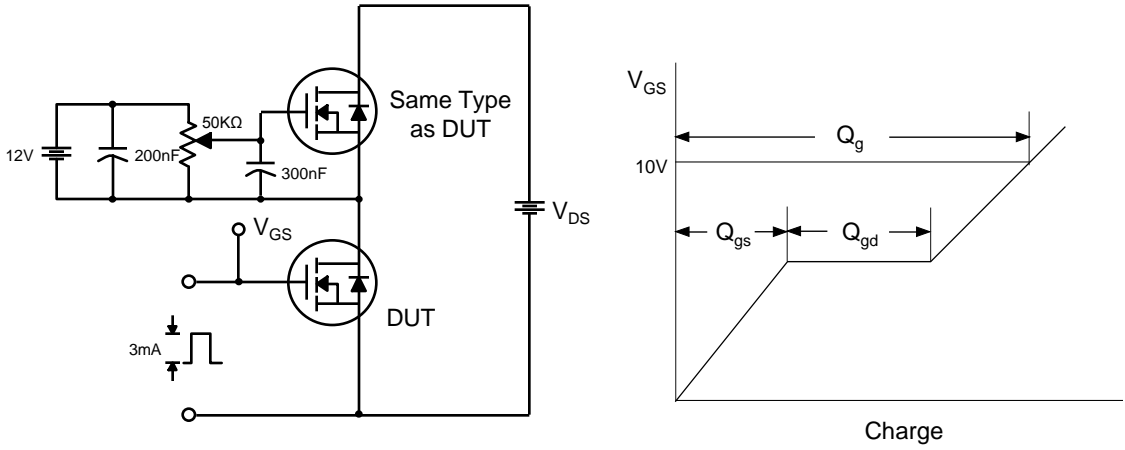


Fig 13. Resistive Switching Test Circuit & Waveforms

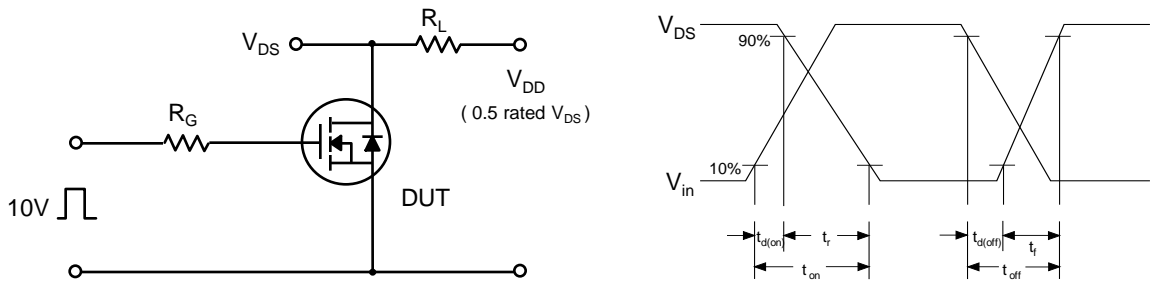


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

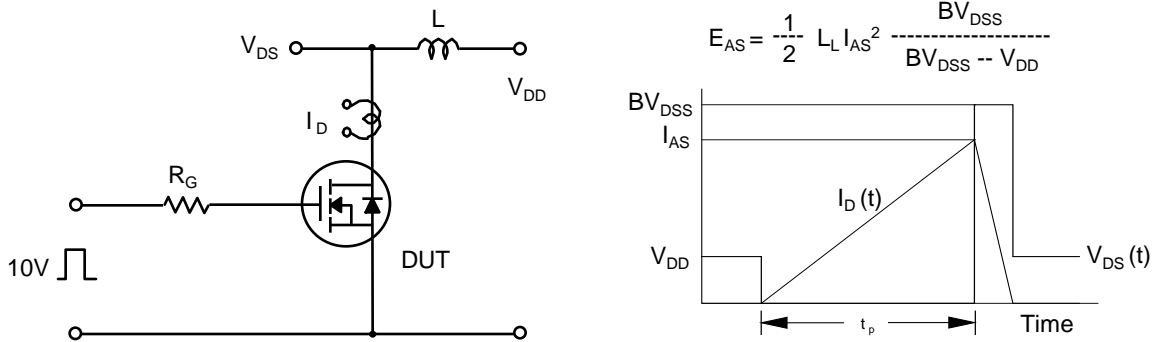
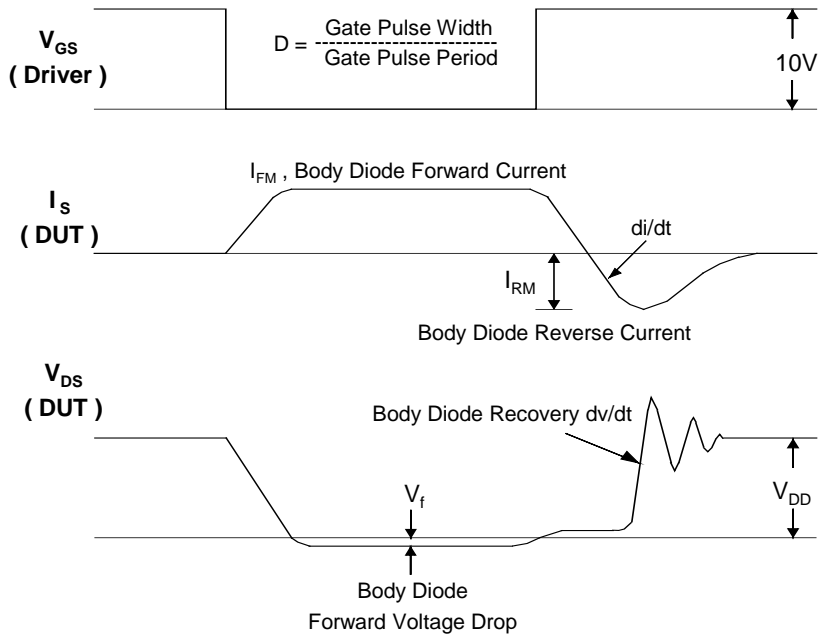
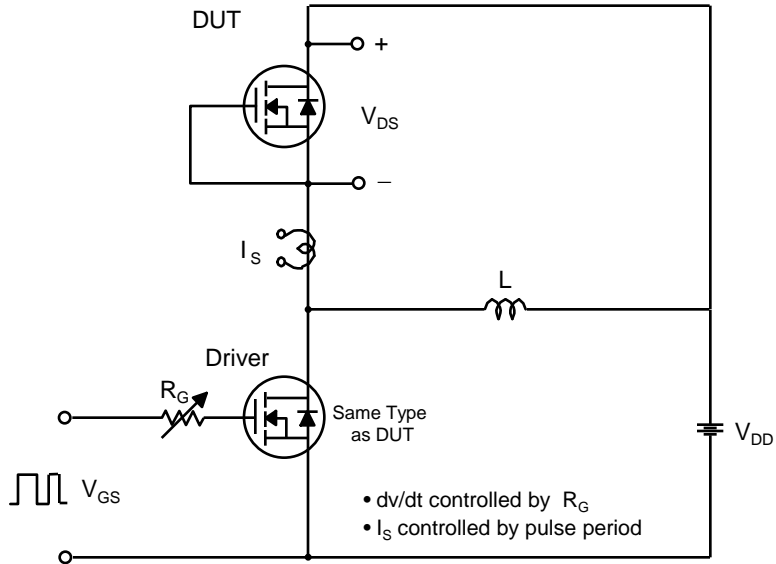
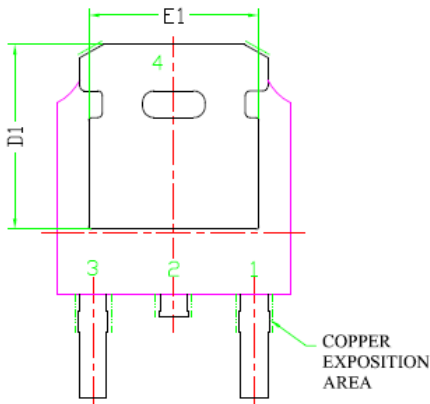
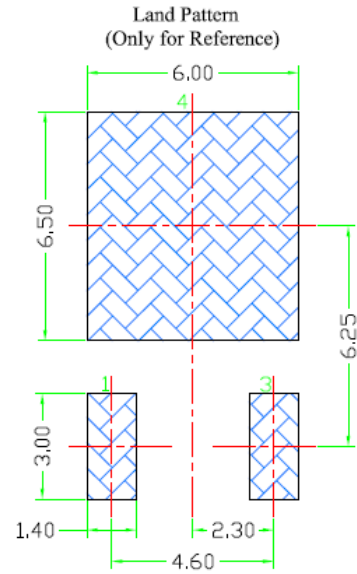
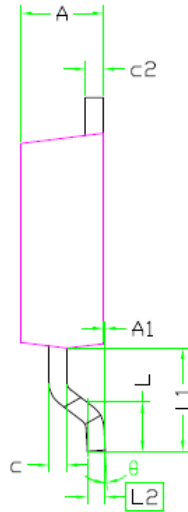
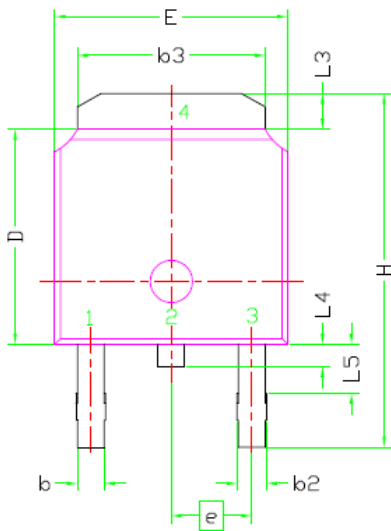


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

D-PAK
(TO-252A)



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
E	6.40	6.60	6.731
L	1.40	1.52	1.77
L1	2.743 REF		
L2	0.508 BSC		
L3	0.89	--	1.27
L4	0.64	--	1.01
L5	--	--	--
D	6.00	6.10	6.223
H	9.40	10.00	10.40
b	0.64	0.76	0.88
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
e	2.286 BSC		
A	2.20	2.30	2.38
A1	0	--	0.127
c	0.45	0.50	0.60
c2	0.45	0.50	0.58
D1	5.21	--	--
E1	4.40	--	--
θ	0°	--	10°