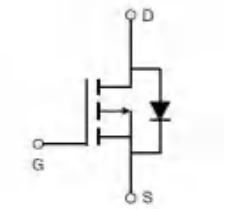
AP50P20Q

P-Channel Enhancement Mosfet

DATA SHEET

Feature

- -20V,-50A
  $R_{DS(ON)}$ <8.5mΩ @V_{GS}=4.5V
  $R_{DS(ON)}$ <12mΩ @V_{GS}=2.5V
- Advanced Trench Technology
- Lead free product is acquired
- Excellent $R_{DS(ON)}$ and Low Gate Charge



Schematic Diagram

Application

- PWM applications
- Load Switch
- Power management

Marking and pin Assignment

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
50P20Q	AP50P20Q	PDFN3X3	13 inch	-	5000

ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	±12	V
Continuous Drain Current (T_a =25℃)	I_D	-50	A
Continuous Drain Current (T_a =100℃)	I_D	-32	A
Pulsed Drain Current (1)	I_{DM}	-200	A
Single Pulsed Avalanche Energy (4)	E_{AS}	44	mJ
Power Dissipation	P_D	50	W
Thermal Resistance from Junction to Case	$R_{\theta JC}$	3.0	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55~ +150	℃

MOSFET ELECTRICAL CHARACTERISTICS(T_a=25℃ unless otherwise noted)

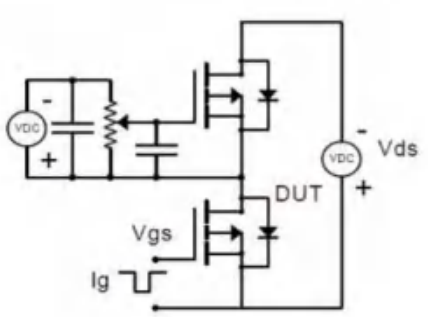
Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	-20	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS} =-20V, V_{GS} = 0V	-	-	1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±12V, V_{DS} = 0V	-	-	±100	nA
Gate threshold voltage(2)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	0.35	0.65	1.0	V
Drain-source on-resistance(2)	$R_{DS(on)}$	V_{GS} =-4.5V, I_D =-20A	-	6.6	8.5	mΩ
		V_{GS} =-2.5V, I_D =-10A	-	8	12	
Dynamic characteristics						
Input Capacitance	C_{iss}	V_{DS} =-10V, V_{GS} =0V, f =1MHz	-	4590	-	pF
Output Capacitance	C_{oss}		-	505	-	
Reverse Transfer Capacitance	C_{rss}		-	440	-	
Switching characteristics						
Turn-on delay time	$t_{d(on)}$	V_{DD}=-10V, I_D=-15A, R_L=3Ω V_{GS}=-10V, R_G=3Ω	-	8	-	ns
Turn-on rise time	t_r		-	59	-	
Turn-off delay time	$t_{d(off)}$		-	111	-	
Turn-off fall time	t_f		-	43	-	
Total Gate Charge	Qg	VDS=-10V, ID=-15A, VGS=-4.5V	-	46	-	nC
Gate-Source Charge	Qgs		-	7.3	-	
Gate-Drain Charge	Qgd		-	10	-	
Source-Drain Diode characteristics						
Diode Forward voltage(2)	V_{DS}	V_{GS} =0V, I_S=-20A	-	-	-1.2	V
Diode Forward current(3)	I_S		-	-	-50	A

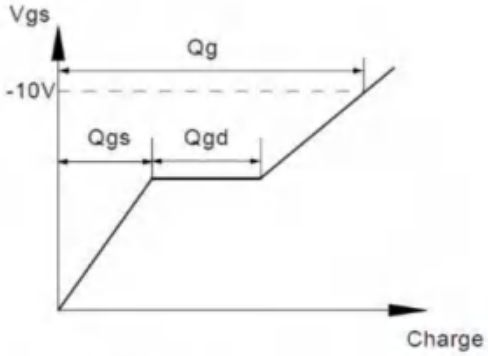
Notes:

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. Pulse Test: pulse width≤300μs, duty cycle≤2%
3. Surface Mounted on FR4 Board,t≤10 sec
4. EAS Condition:T_J=25℃,V_{DD}=-10V,R_G=25Ω,L=0.5mH

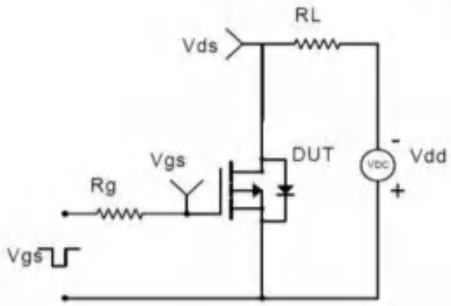
Test Circuit

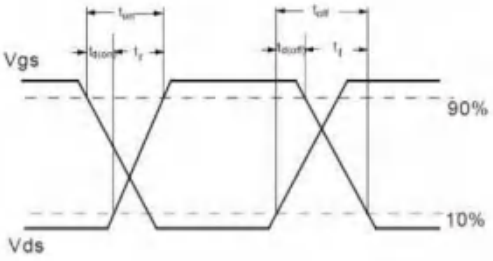
Gate Charge Test Circuit & Waveform



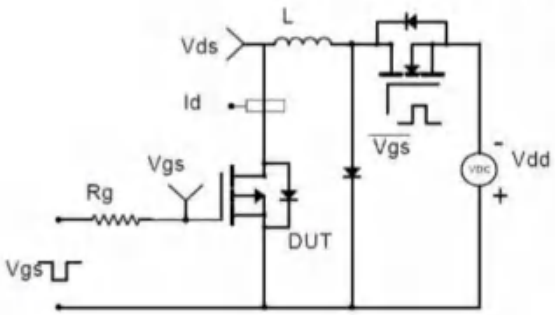


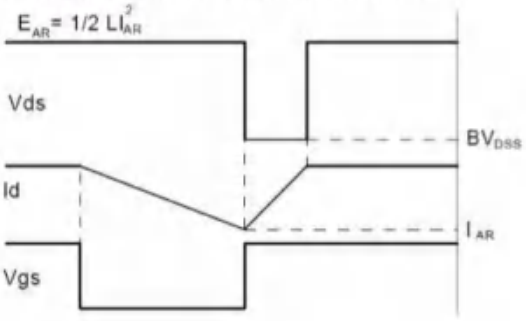
Resistive Switching Test Circuit & Waveforms



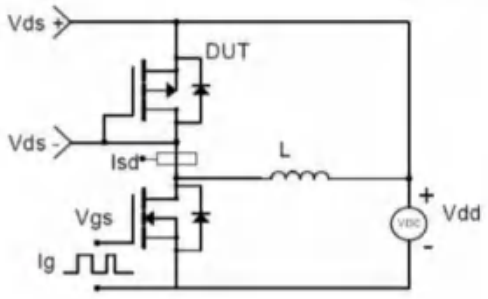


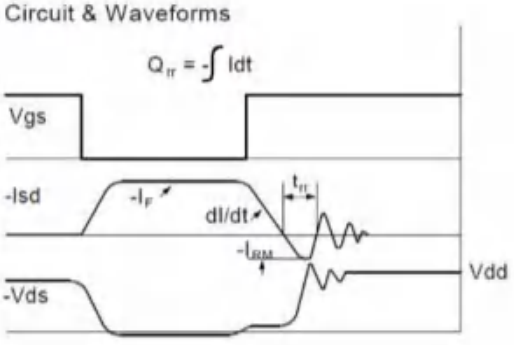
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms





Typical Performance Characteristics

Figure1: Output Characteristics

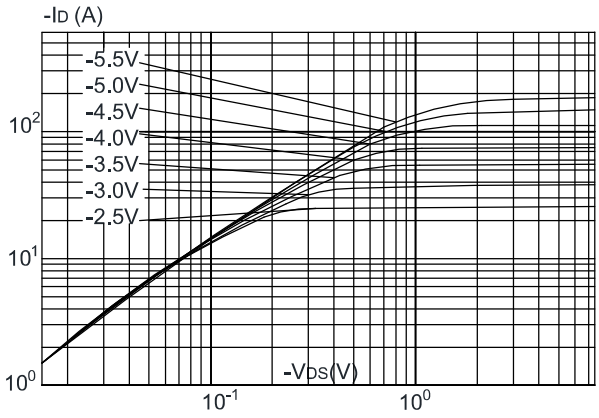


Figure 2: Typical Transfer Characteristics

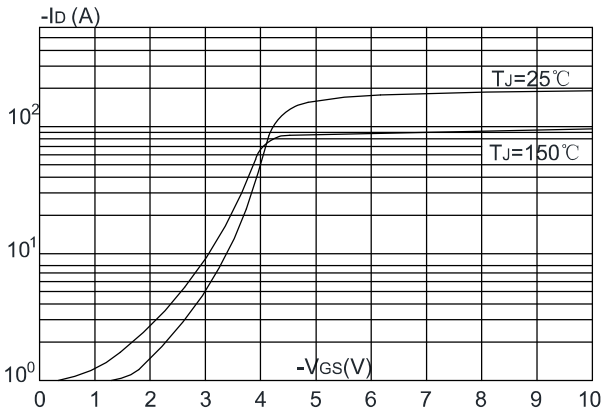


Figure 3: On-resistance vs. Drain Current

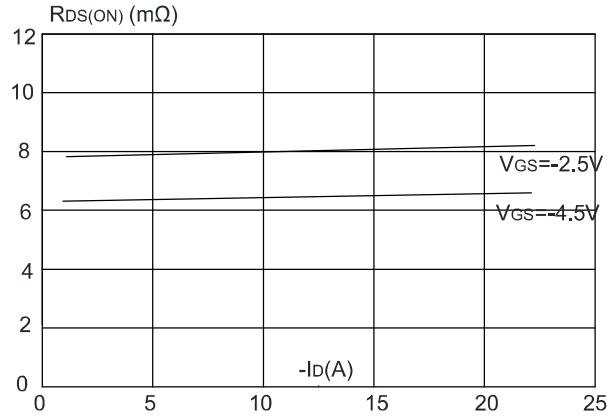


Figure 4: Body Diode Characteristics

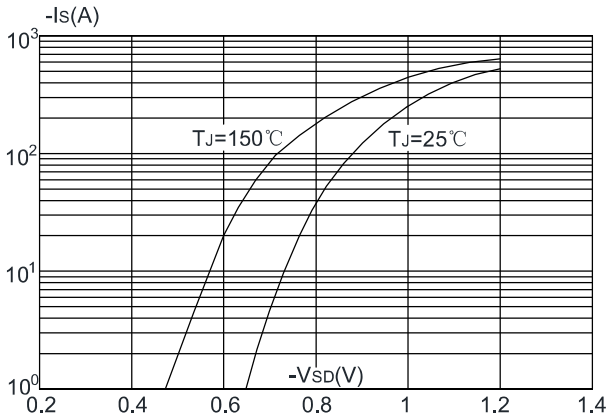


Figure 5: Gate Charge Characteristics

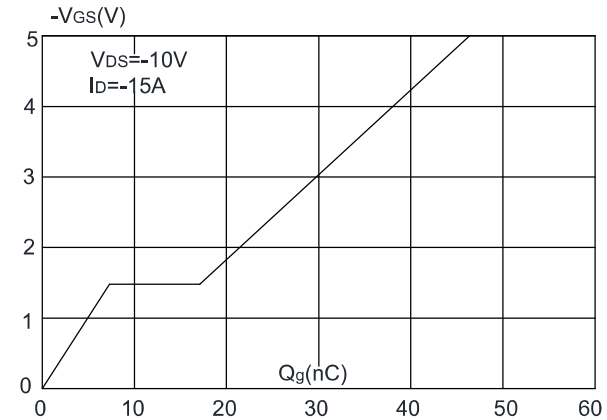


Figure 6: Capacitance Characteristics

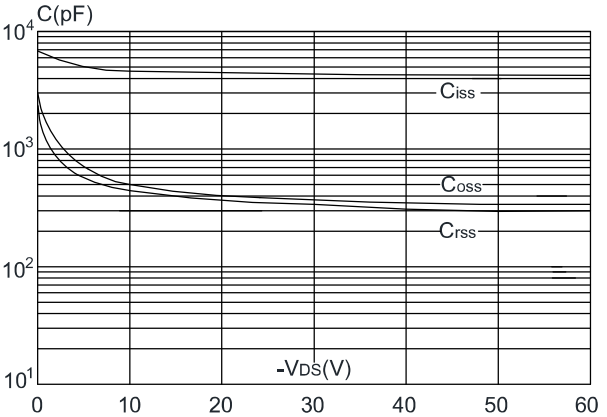


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

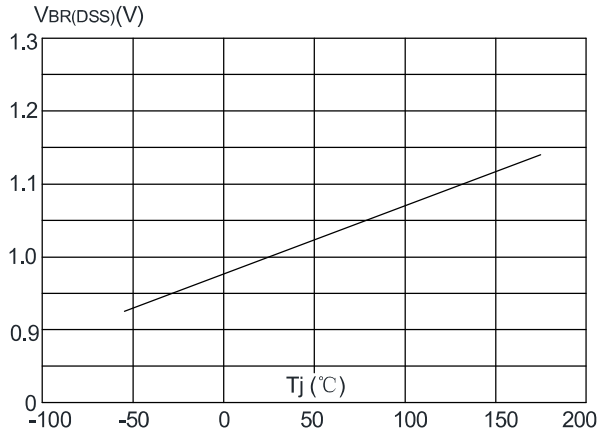


Figure 8: Normalized on Resistance vs. Junction Temperature

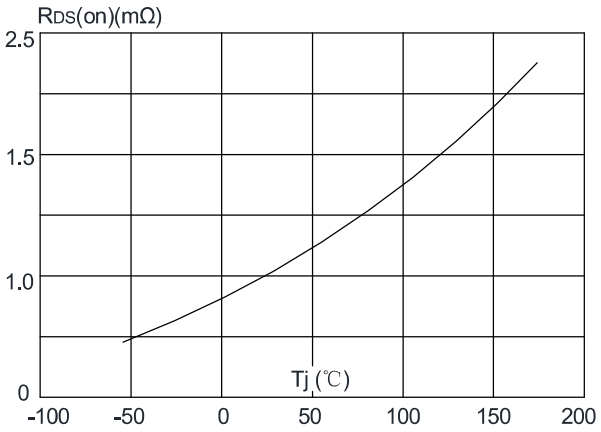


Figure 9: Maximum Safe Operating Area

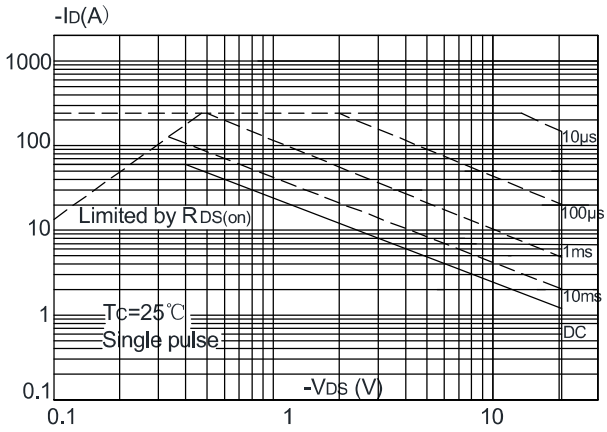


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

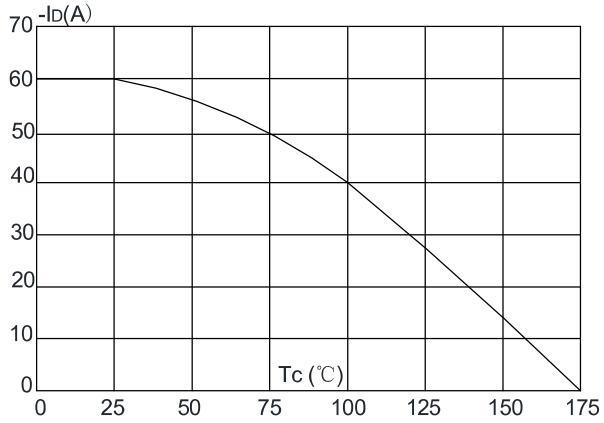
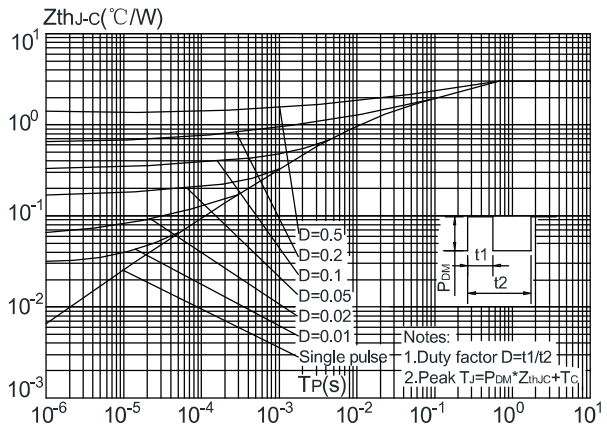
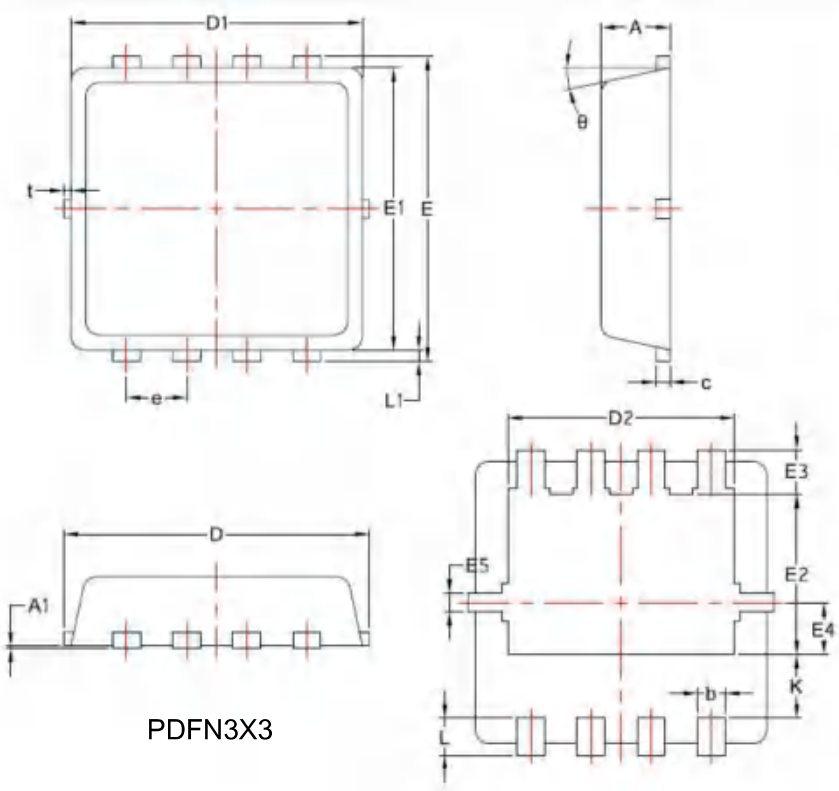


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Package Mechanical Data



PDFN3X3

SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
θ	10°	12°	14°