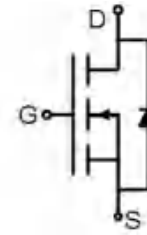


Feature

- 40V,54A
 $R_{DS(ON)} < 6.8m\Omega @ V_{GS}=10V$ (TYP:5.7m Ω)
 $R_{DS(ON)} < 11m\Omega @ V_{GS}=4.5V$ (TYP:8.5m Ω)
- Split Gate Trench Technology
- Lead free product is acquired
- Excellent $R_{DS(ON)}$ and Low Gate Charge



Schematic Diagram

Application

- PWM applications
- Load Switch
- Power management



Marking and pin Assignment

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
G068N04Q	APG068N04Q	PDFN3X3	13 inch	-	5000

ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_a=25^\circ\text{C}$)	I_D	54	A
Continuous Drain Current ($T_a=100^\circ\text{C}$)	I_D	34	A
Pulsed Drain Current ⁽¹⁾	I_{DM}	216	A
Single Pulsed Avalanche Energy ⁽²⁾	E_{AS}	56	mJ
Power Dissipation	P_D	36.7	W
Thermal Resistance from Junction to Case	$R_{\theta JC}$	3.4	$^\circ\text{C}/\text{W}$
Junction Temperature	T_J	175	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55~ +175	$^\circ\text{C}$

MOSFET ELECTRICAL CHARACTERISTICS($T_a=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	40	-	-	V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 40V, V_{GS} = 0V$	-	-	1	μA
Gate-body leakage current	I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	± 100	nA
Gate threshold voltage ⁽³⁾	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	1.6	2.0	V
Drain-source on-resistance ⁽³⁾	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$	-	5.7	6.8	m Ω
		$V_{GS} = 4.5V, I_D = 15A$	-	8.5	11	
Gate Resistance	R_g	$V_{DS} = V_{GS} = 0V, f = 1MHz$	-	3.6	-	Ω
Dynamic characteristics						
Input Capacitance	C_{iss}	$V_{DS} = 20V, V_{GS} = 0V, f = 1MHz$	-	840	-	pF
Output Capacitance	C_{oss}		-	254	-	
Reverse Transfer Capacitance	C_{rss}		-	5	-	
Switching characteristics						
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20V, I_D = 20A, V_{GS} = 10V, R_G = 10\Omega$	-	4	-	ns
Turn-on rise time	t_r		-	11	-	
Turn-off delay time	$t_{d(off)}$		-	25	-	
Turn-off fall time	t_f		-	23	-	
Total Gate Charge	Q_g	$V_{DS} = 20V, I_D = 20A, V_{GS} = 4.5V$	-	13.1	-	nC
Gate-Source Charge	Q_{gs}		-	2.2	-	
Gate-Drain Charge	Q_{gd}		-	2.6	-	
Reverse Recovery Chrage	Q_{rr}	$I_F = 40A, di/dt = 100A/us$	-	5.8	-	nC
Reverse Recovery Time	T_{rr}	$I_F = 40A, di/dt = 100A/us$	-	18	-	ns
Source-Drain Diode characteristics						
Diode Forward voltage ⁽³⁾	V_{DS}	$V_{GS} = 0V, I_S = 50A$	-	-	1.2	V
Diode Forward current ⁽⁴⁾	I_S		-	-	54	A

Notes:

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition: $T_J = 25^{\circ}\text{C}, V_{DD} = 20V, R_G = 25\Omega, L = 0.5mH$
3. Pulse Test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
4. Surface Mounted on FR4 Board, $t \leq 10\text{ sec}$

Test Circuit

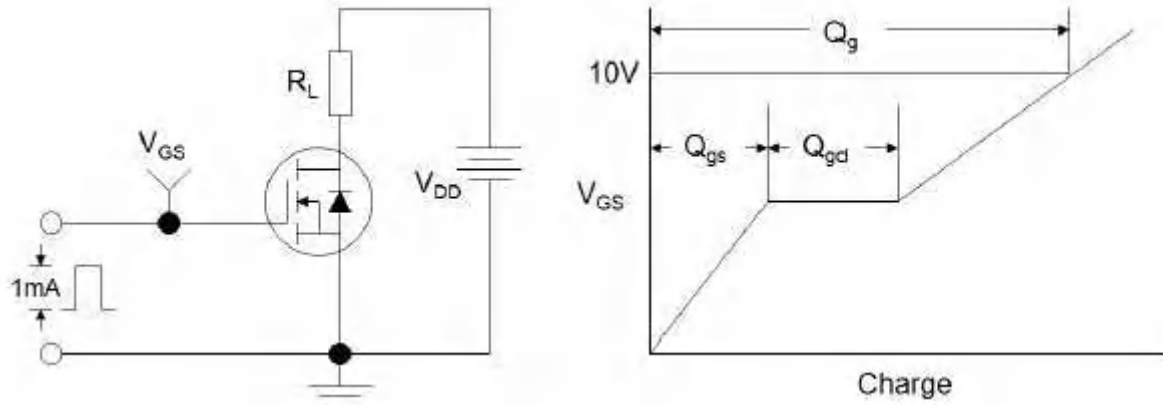


Figure1:Gate Charge Test Circuit & Waveform

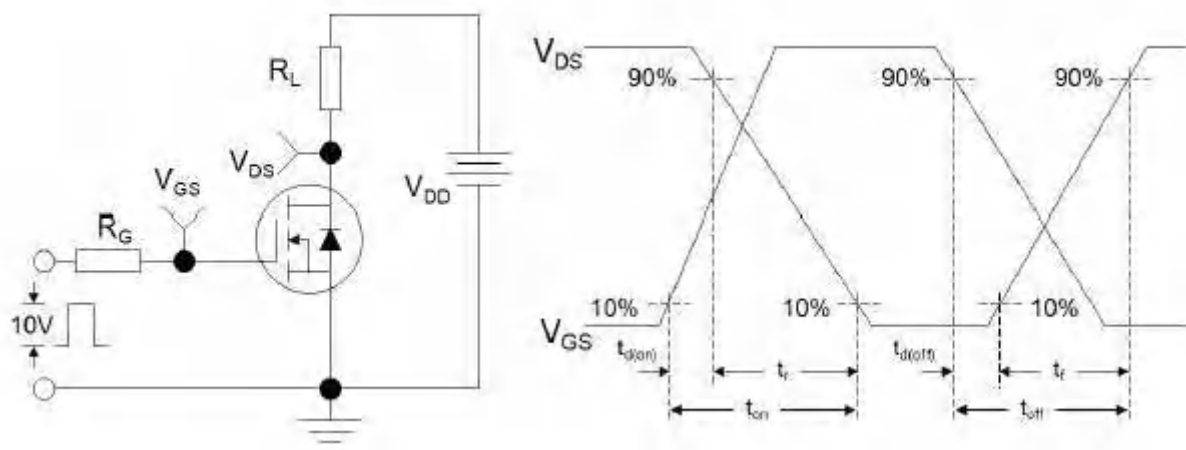


Figure 2: Resistive Switching Test Circuit & Waveforms

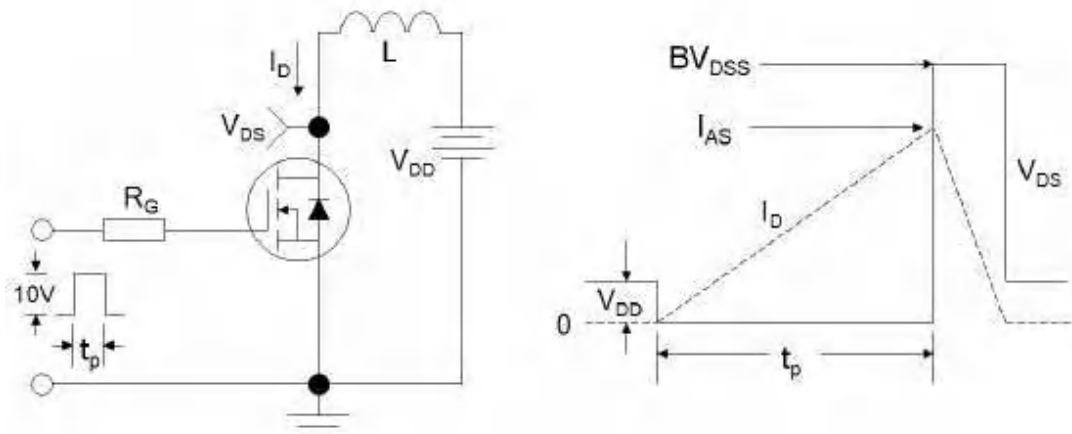
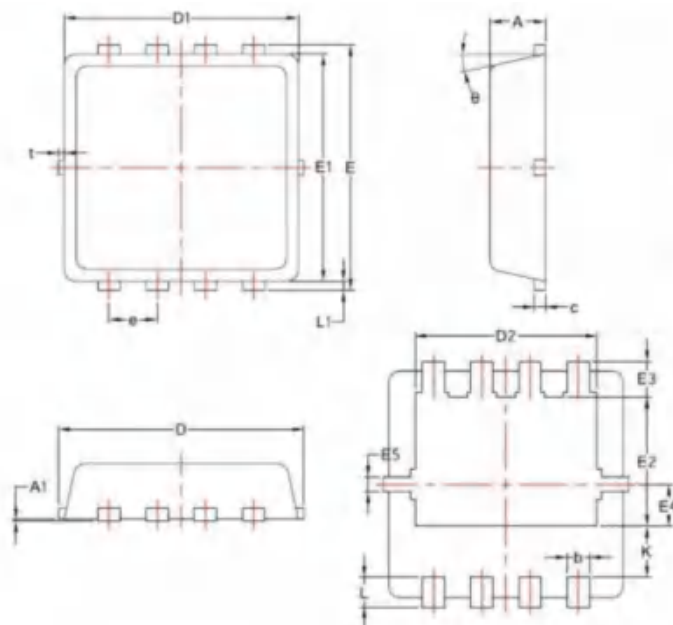


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

APG068N04Q
N-Channel Enhancement Mosfet

PDFN3X3 Package Information



SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
θ	10°	12°	14°