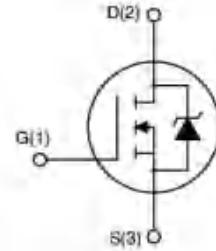


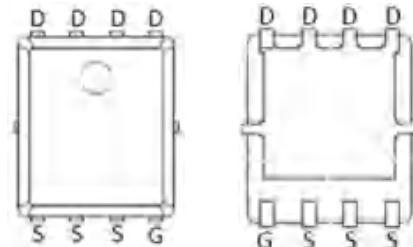
Feature

- 100V,60A
- $R_{DS(on)} < 9.5\text{ m}\Omega$ @ $V_{GS}=10\text{ V}$ (TYP: $8.2\text{ m}\Omega$)
- $R_{DS(on)} < 13\text{ m}\Omega$ @ $V_{GS}=4.5\text{ V}$ (TYP: $11.3\text{ m}\Omega$)
- Split Gate Trench Technology
- Lead free product is acquired
- Excellent $R_{DS(on)}$ and Low Gate Charge



Application

- PWM applications
- Load Switch
- Power management



PDFN5X6-8L

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
G095N01G	APG095N01G	PDFN5*6-8L	13 inch	-	5000

ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_a = 25^\circ\text{C}$)	I_D	60	A
Continuous Drain Current ($T_a = 100^\circ\text{C}$)	I_D	38	A
Pulsed Drain Current ⁽¹⁾	I_{DM}	240	A
Singel Pulsed Avalanche Energy ⁽²⁾	E_{AS}	90	mJ
Power Dissipation	P_D	63	W
Thermal Resistance from Junction to Case	R_{eJC}	2.0	$^\circ\text{C}/\text{W}$
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55~+150	$^\circ\text{C}$

APG095N01G

N-Channel Enhancement Mosfet

MOSFET ELECTRICAL CHARACTERISTICS($T_a=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100	-	-	V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 80V, V_{GS} = 0V$	-	-	1	μA
Gate-body leakage current	I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	± 100	nA
Gate threshold voltage ⁽³⁾	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.2	2.0	2.5	V
Drain-source on-resistance ⁽³⁾	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$	-	8.2	9.5	$m\Omega$
		$V_{GS} = 4.5V, I_D = 10A$	-	11.3	13	
Forward Threshold Voltage	g_{fs}	$V_{DS} = 5V, I_D = 20A$	-	13.5	-	S
Gate Resistance	R_g	$V_{DS} = V_{GS} = 0V, f = 1MHz$	-	1.94	-	Ω
Dynamic characteristics						
Input Capacitance	C_{iss}	$V_{DS} = 50V, V_{GS} = 0V, f = 1MHz$	-	2122	-	pF
Output Capacitance	C_{oss}		-	618	-	
Reverse Transfer Capacitance	C_{rss}		-	25	-	
Switching characteristics						
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 50V, I_D = 20A,$ $V_{GS} = 10V, R_G = 3\Omega$	-	17	-	ns
Turn-on rise time	t_r		-	4	-	
Turn-off delay time	$t_{d(off)}$		-	32	-	
Turn-off fall time	t_f		-	8	-	
Total Gate Charge	Q_g	$V_{DS} = 50V, I_D = 20A,$ $V_{GS} = 10V$	-	41.8	-	nC
Gate-Source Charge	Q_{gs}		-	9	-	
Gate-Drain Charge	Q_{gd}		-	10	-	
Reverse Recovery Charge	Q_{rr}	$I_F = 20A, di/dt = 100A/us$		71.5		nC
Reverse Recovery Time	T_{rr}	$I_F = 20A, di/dt = 100A/us$		50.5		ns
Source-Drain Diode characteristics						
Diode Forward voltage ⁽³⁾	V_{DS}	$V_{GS} = 0V, I_S = 20A$	-	-	1.2	V
Diode Forward current ⁽⁴⁾	I_S		-	-	60	A

Notes:

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition: $T_J = 25^\circ C, V_{DD} = 50V, R_G = 25\Omega, L = 0.5mH$
3. Pulse Test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
4. Surface Mounted on FR4 Board, $t \leq 10$ sec

Typical Performance Characteristics

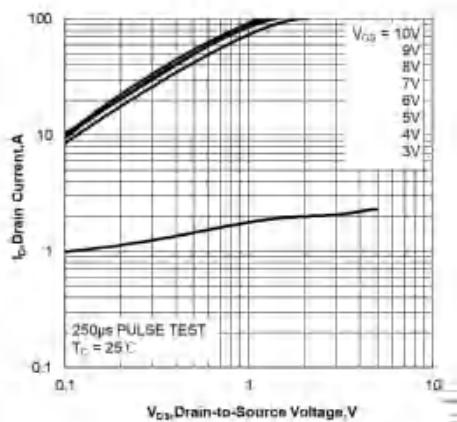


Figure 1. Output Characteristics

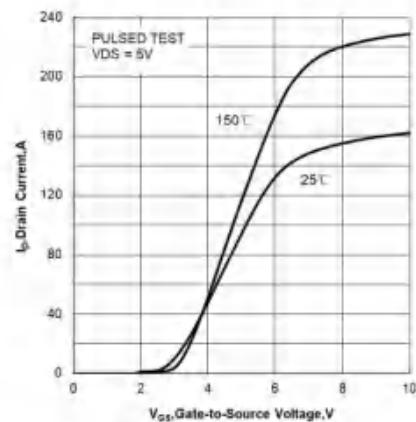


Figure 2. Transfer Characteristics

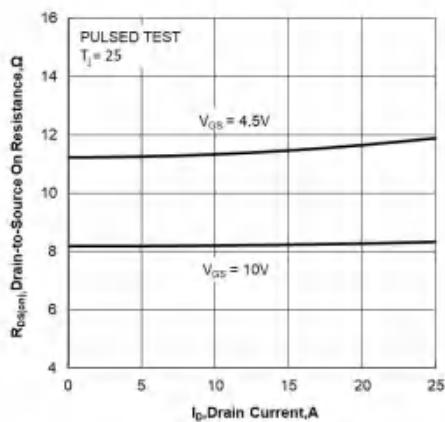


Figure 3. Drain-to-Source On Resistance
vs Drain Current

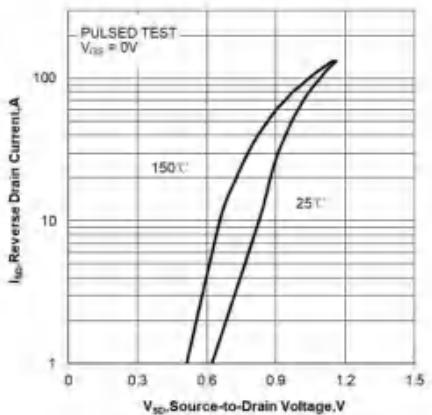


Figure 4. Body Diode Forward Voltage
vs Source Current and Temperature

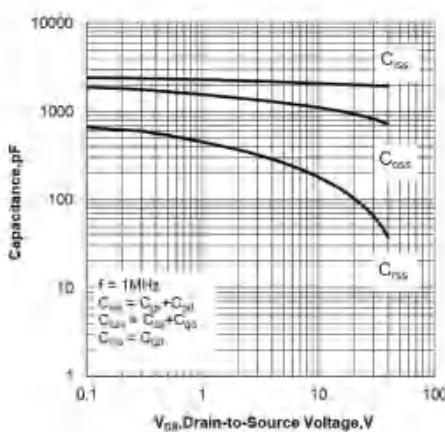


Figure 5. Capacitance Characteristics

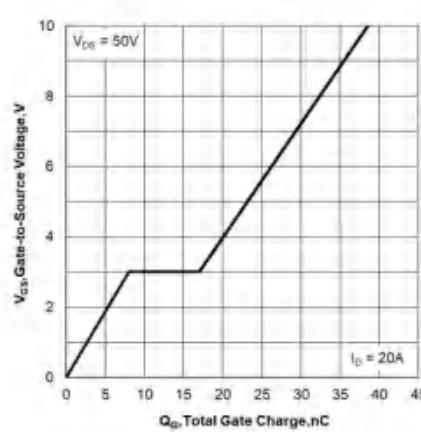
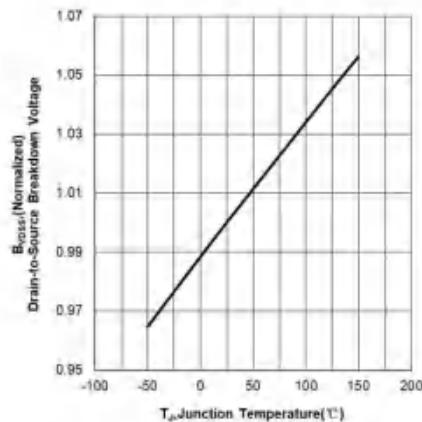


Figure 6. Gate Charge Characteristics

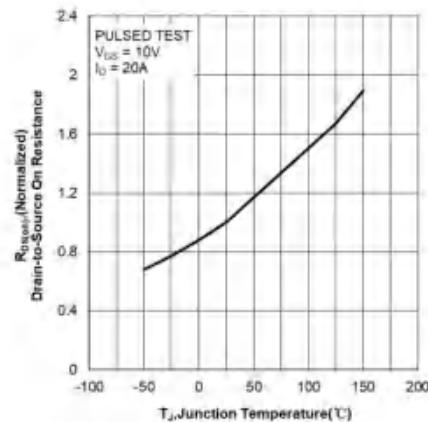
APG095N01G

N-Channel Enhancement Mosfet

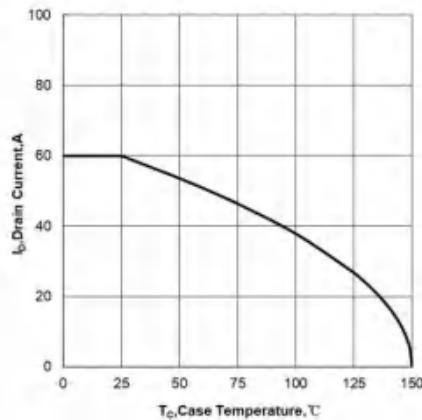
AllPOWER
DATA SHEET



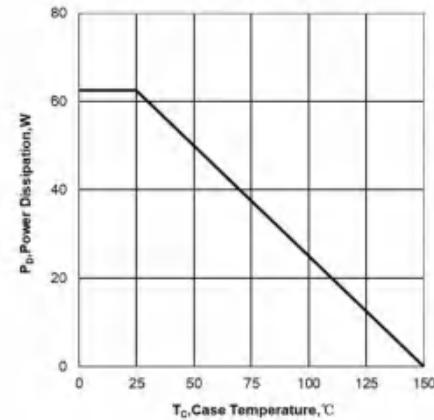
**Figure 7. Normalized Breakdown Voltage
vs Junction Temperature**



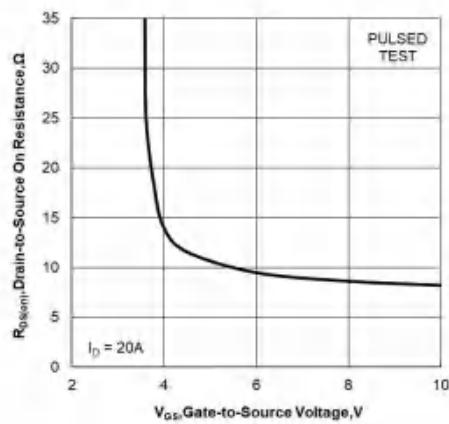
**Figure 8. Normalized On Resistance vs
Junction Temperature**



**Figure 9. Maximum Continuous Drain Current
vs Case Temperature**



**Figure 10. Maximum Power Dissipation
vs Case Temperature**



**Figure11. Drain-to-Source On Resistance vs Gate
Voltage and Drain Current**

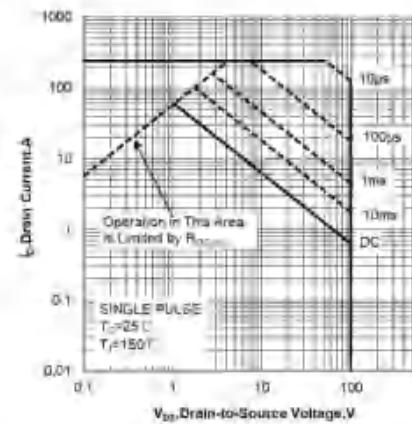


Figure 12. Maximum Safe Operating Area

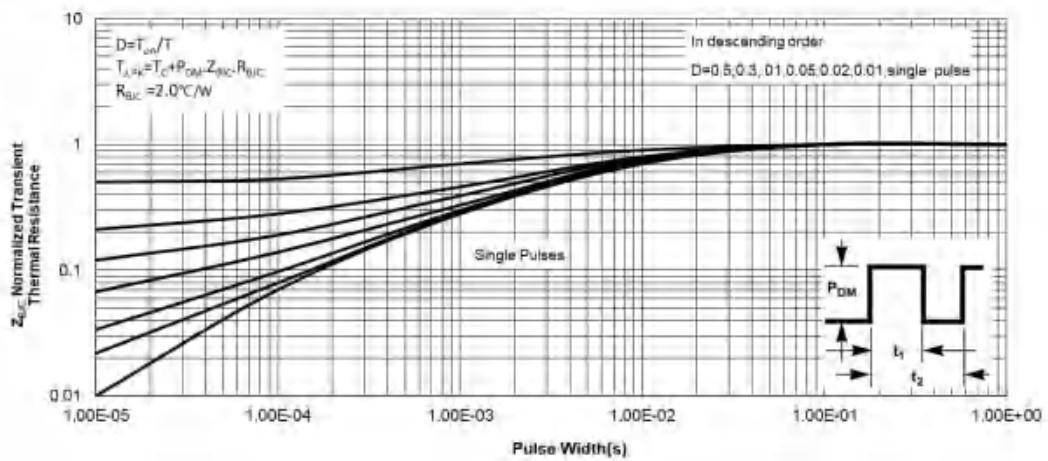
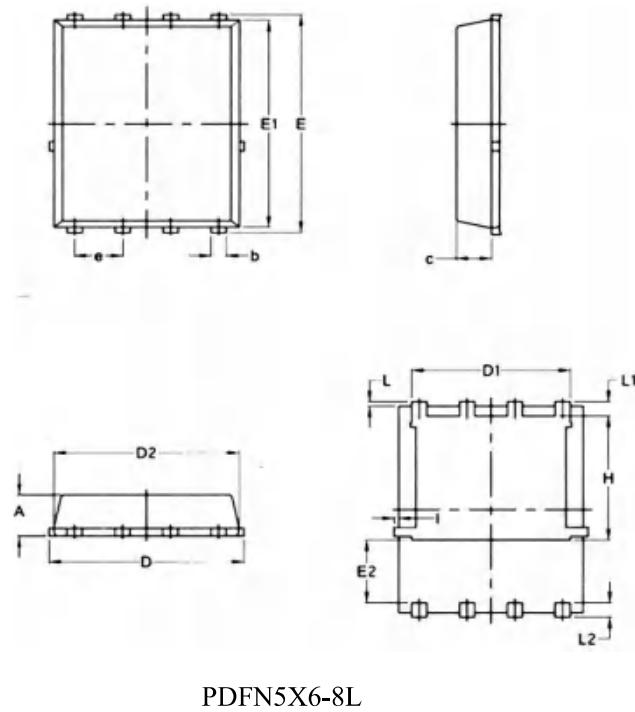


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

PDFN5*6-8L Package Information



S Y M B O L	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.970	0.0324	0.0382
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	—	0.0630	—
e	1.27	BSC	0.05	BSC
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	—	0.18	—	0.0070